In the Claims:

1-34. (canceled)

35. (previously amended) An integrated circuit comprising:

A. a substrate of semiconductor material;

B. pads formed on the semiconductor material;

C. functional circuits formed on the substrate and having functional output leads coupled to the pads;

D. output buffer circuitry formed on the substrate, for each functional output lead, the buffer circuitry having a buffer input lead connected to the functional output lead and having a buffer output lead connected to a pad;

E. test access port circuitry formed on the substrate, the test access port circuitry having a test data input lead, a test data output lead, a test clock input lead, and a test mode select input lead, all connected to the pads;

F. scan cells formed on the substrate and connected to the test access port circuitry, to the test data input lead, and to the test data output lead;

G. test leads formed on the substrate and connected to the pads; and

H. scannable switch circuitry formed on the substrate and connected to the test access port circuitry, to the test data input lead, and to the test data output lead, the scannable switch circuitry selectively connecting a buffer input lead and a buffer output lead to the test leads, the scannable switch circuitry including a multiplexer, which has an output connected to the input of a capture-shift memory, which has an output connected to the input of an update memory, which has an output connected to a switch, the switch being connected in series between a buffer lead and a test lead, the multiplexer having an input connected to the test data input lead and the output of the capture-store memory being connected to the test data output lead,

there being one scannable switch circuitry selectively connecting one buffer lead to one test lead.

36. (canceled)

37. (canceled)

38. (previously presented) The integrated circuit of claim 35 in which the test leads are input leads and output leads.

39. (previously presented) The integrated circuit of claim 35 in which a scan cell selectively connects a functional output lead to the buffer input lead.

40. (previously presented) The integrated circuit of claim 35 including a bus hold circuit connected to the buffer output lead.

41. (previously presented) The integrated circuit of claim 35 including an electrostatic discharge circuit connected to the buffer output lead.

42. (previously presented) The integrated circuit of claim 35 including a bus hold circuit and an electrostatic discharge circuit connected to the buffer output lead.